REMARKS

Thirty claims were originally filed in this case, and all claims were rejected. Please cancel claims 1-9 and 25-30. Claims 10, 14, 16, 17, 19, 20 and 21 have been amended. Reconsideration of the application in view of the above changes and the following remarks is respectfully requested.

During the preparation of this amendment, the Applicant noticed a number of typographical and other minor errors in the specification and drawings. The Applicant has amended the specification and drawings as identified above to correct the errors noted. Applicant submits that no new matter is added by these changes to the specification and drawings.

Corrections for Consistency and §112, Second Paragraph

In paragraph 1 on page 2 of the Office Action, the Examiner noted a number of instances where the claims needed correction such that the claims particularly point out and distinctly claim what applicants regard as the invention, as well as remove ambiguities in the claims. In particular, the Examiner noted the following:

As per claim 14, line 4, "one of the plurality of registers in the register" is unclear as to the precise scope and meaning of the language. Claims 14 has been amend to clarify this language.

As per claim 16, "the load instruction unit" lacks proper antecedent basis. Claim 16 has been amended to provide proper antecedent basis for this term.

As per claim 17, "the address offsets" lacks proper antecedent basis. Claim 17 has been amended to provide proper antecedent basis for this term.

As per claim 19, "the address bit shifter" lacks proper antecedent basis. Claim 19 has been amended to provide proper antecedent basis for this term.

As per claim 20, "the fetch logic unit" lacks proper antecedent basis. Claim 20 has been amended to provide proper antecedent basis for this term.

As per claim 21, "the partition look-up table" lacks proper antecedent basis. Claim 21 has been amended to provide proper antecedent basis for this term.

Applicant has amended the above claims to remove and correct the inconsistencies noted by the Examiner. Applicant believes that with the above amendments, the claims no longer have any objectionable or ambiguous language.

Election/Restriction

In paragraphs 2-4 of the Office Action, the Examiner noted that the amendment to the claims did not obviate the need for a restriction, and that complete reply to the final rejection must include cancellation of non-elected claims. With this amendment, Applicant has canceled Claims 1-9 and 25-30.

Rejection of the Claims under 35 U.S.C. §§ 102 and 103

In paragraph 6 of the Office Action, the Examiner rejected claims 10-20 under 35 U.S.C. § 102(e) as being anticipated by Larson et al (U.S. Pat. No. 5,793,386 and hereinafter "Larson"). The Examiner contends that Larson teaches a graphics system for processing parameter values of graphics primitives in a display list, the graphics system comprising a plurality of register files for storing a plurality of parameter values representing graphics primitives defined in the display list; and a graphics processor coupled to the plurality of register

files, wherein the graphics processor generates and processes a shortened display list to enable faster processing of the graphics primitives, while maintaining the display quality of primitives displayed in a display unit.

In paragraph 8 of the Office Action, the Examiner rejected claims 21-24 under 35 U.S.C. § 103(a) as being unpatentable over Larson et al. In particular, the Examiner believes that Larson discloses as noted above, but fails to explicitly teach the partition look-up table comprises 64 entries of address offsets to the register file. However, the Examiner submits that it would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Larson et al because the number of entries for the table are always power of 2 and to choose 64 is merely a matter of design choice.

Applicants have amended claim 10 to more clear define the novel aspects of the claimed invention. In particular, claim 10 as amended now recites:

> A graphics system for processing parameter values of graphics primitives in a display list, wherein the display list is shortened to enable fast processing time while maintaining the quality of information contained in the display list, the graphics system comprising:
>
> a plurality of register files for storing a plurality of parameter values representing graphics primitives defined in the display list; and
>
> a graphics processor coupled to the plurality of register files, wherein the graphics processor processes the **shortened display list** while maintaining the display quality of primitives displayed in a display unit, the graphics processor processing **load instructions representative of a shortened display list instruction including the fetching of parameters associated with the shortened display list instruction and storing fetched parameters randomly in the plurality of register files.** (Emphasis added).

Applicant submits that as amended claim 10 is patentably distinct over the art of record. Claim 10 now recites the novel aspects of the present invention including a graphics processor that is able to process shortened display list instructions when loading the register files. Such a novel structure is not taught or suggested by any of the art of record.

The claimed invention is particularly advantageous because it provides a method for using the host processor to store data in an efficient manner in the register file of the graphics subsystem. Before the claimed invention, the system had to either unnecessarily load registers in the register file, or divide a single load instruction into multiple load instructions. In either case, the transmission of data over the system bus 101 was not as efficient as possible, and therefore affected the overall performance of the system as well as the performance of the graphics subsystem. In the former case, data is transmitted over the bus which is not necessary. In the later case, the overhead of the additional instructions makes not needing to send certain parameter values offset each other. However, the claimed invention provides an elegant solution in which a relatively small and inexpensive amount of logic in the form of fetch subsequent instruction and a load instruction unit are added such that the operations by the host computer can be utilized to increase the efficiency of transferring graphic data from main memory to the graphics subsystem. The present invention provides the capability to handle special load instructions in which only the necessary parameter values associated with a graphics primitive are loaded from the main memory to the register files. Since the bottle neck is often memory and the system bus, the claimed invention reduces the bandwidth constraints of these devices by allowing special operations to the register file of the graphics subsystem. The prior art is absent any similar teaching.

Applicant submits that the claimed invention is not anticipated or rendered obvious by Larson. Larson discloses a graphic system as has been noted above by the Examiner. However, Larson fails to teach the graphics processor of the claimed invention wherein the graphics processor processes load instructions representative of a shortened display list instruction including the fetching of parameters associated with the shortened display list instruction and

storing fetched parameters randomly in the plurality of register files. There is no discussion or even contemplation of shortened display list instruction in Larson, or the processor as claimed which selectively loads into the register file only the necessary parameter for the primitive.

Applicant submits that the claimed invention is not shown by Larson for a number of reasons. First, the lack of similar structure as noted above including the processor that retrieves and stores only the necessary values for the primitive, thereby minimizing the data required to pass over the system bus. Second, the invention of Larson is directed to a system/method that solves a different problem of rending the data after it is in the register file and what data to pass from the register file to the rendering engine. The invention of Larson is in fact complementary to the claimed invention. Such an invention could be used in conjunction with the claimed invention to make the system even faster. Larson is directed to improving the communication path from the register file to the rendering engine and does so by skipping certain parameter values and only passing certain necessary ones according to the type of primitive to render (See col. 14, lns. 9-14). In contrast, the claimed invention is directed to improving the loading of the data into the register file in a more efficient manner. The claimed invention focuses on the path from the main memory to the register file, and not the path from the register file to the rendering engine. Third, the disclosure of Larson does not suggest or contemplate use of a partition look-up table to generate the addresses to the register file. Finally, Larson has no suggestion of unique instruction format that provides the instruction, the parameters to load (e.g., the write enable) an the partition address. Therefore, Applicant submits that claim 10 is patentably distinct over Larson.

Claims 11-24 depend, either directly or indirectly from claim 10. Claims 11-24 also include recitations that further defined the claimed invention such as but not limited to

instruction fetch logic unit, a load instruction unit and a partition table. Based on their dependence on claim 10 and other patentable recitations, claims 11-24 are also believed to be patentable.

Applicant respectfully requests a two-month extension of time in responding to the above-identified office action and has also enclosed a check for the requisite fee for the two-month extension of time in responding to the above-identified office action.

In view of the foregoing arguments, Applicant respectfully submits that the claims presently in this case are now in condition for allowance. Reconsideration and prompt favorable action are therefore solicited.

Respectfully submitted,
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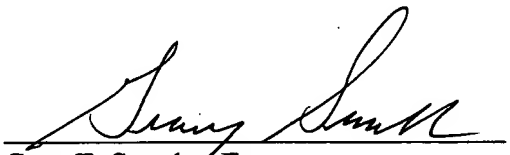
By: 

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